REMARKS

Claims 1-24 are presently pending in this application. Claims 1, 5, and 14 have been amended to more particularly define the invention. It is noted that the claim amendments are made only to assure grammatical and idiomatic English and improved form under United States practice, and are not made to distinguish the invention over the prior art or narrow the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1 and 4 were rejected under 25 U.S.C. §102(b) as being anticipated by Nagano, U.S. Patent No. 5,687,003. Claims 14-17 and 24 were rejected under 35 U.S.C. §102(e) as being anticipated by Johnson, et al., U.S. Patent No. 6,686,957. Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Nagano in view of Koji, et al. JP08298601 or Murakami, JP401176119. Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano in view of Tani, EP 760,514 A2. Claims 5-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nagano in further view of Hasegawa et al., U.S. Patent No. 5,384,645. Claims 7, 9, 11, and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nagano and Hasegawa in further view of Nagai, U.S. Patent Publication No. 2000/0010561. Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over Nagano, Hasegawa, and Nagai in further view of Kubo, U.S. Patent No. 6,639,626. Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Nagano, Hasegawa, and Nagai, and also as being unpatentable over Nagano, Hasegawa, and Nagai in view of Yoshihiro, JP 11-261871. Claim 12 was rejected under 35 U.S.C. §103(a)

as being unpatentable over Nagano in view of Johnson. Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Hasegawa. Claims 19 and 21-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Nagai. Claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson in further view of Kubo. Claim 23 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson in further view of Nagai and Yoshihiro. These rejections are traversed.

THE CLAIMED INVENTION

The claimed invention is directed to an image sensing apparatus. In an exemplary embodiment, the inventive image sensing apparatus includes an image quality mode setting block for setting only one of a plurality of image quality modes, a solid state image sensing element for converting an optical image into an electric analog signal, and an analog-to-digital (AD) conversion block for converting the analog signal output from the solid state image sensing element into a single digital signal with a quantization bit count corresponding only to the one image quality mode set by the image quality mode setting block.

In another exemplary embodiment, the inventive image sensing apparatus includes an image sensing apparatus which has an image quality mode setting block for setting one of a plurality of image quality modes, a solid state image sensing element for converting an optical image into an electric analog signal, and an AD conversion block for converting the analog signal into a digital signal. The AD conversion block has a plurality of quantization bit counts corresponding respectively to the plurality of image quality modes and is responsive to the image quality mode set by the image quality mode setting block to enable

the quantization bit count corresponding to the set image quality mode and to disable the other quantization bit counts.

THE PRIOR ART REFERENCES

The Nagano Reference

Nagano discloses an optical reader having a high-resolution mode and a high-speed mode. Signals from a CCD sensor 40 are passed through a buffer to a first AD converter 51, which provides a 12-bit, high resolution, output, and to a second AD converter 42, which provides an 8-bit, high-speed, output. The two outputs from the two AD converters are applied to data selector 53 which selects one of the outputs and sends the selected output to control circuit 52.

The Johnson, et al. Reference

Johnson, et al. discloses a preview mode low resolution output system and method in which signals from a CCD sensor 14 are adjusted by a black level adjustment circuit 45, passed through a correlated double sampler and variable gain amplifier circuit 44, and applied to an AD converter 46, the output of which is applied to a gain adjust circuit 47 which performs the reverse operation of the variable gain amplifier.

The Koji, et al. Reference

Koji, et al. discloses a video signal processor in which level-compressed signals are converted into digital video signals with regulated word length. The levels of the video

signals are compressed so that the rate of the resolution of digital video signals is held to a desired level.

The Murakami Reference

Murakami shows a parallel analog-to-digital converter in which the resolution may be set with a switch at a node corresponding to the required resolution.

The Hasegawa Reference

Hasegawa shows an image rotating apparatus which controls write/read addresses every B/N pieces on bringing together input image data having N-bit information per pixel in accordance with a word width B.

The Nagai Reference

Nagai shows an image sensing apparatus and method including a video signal processing circuit which downsamples pixels is such a manner that the number of pixels constituting one frame of an image becomes the number of pixels on an image displayed on a display unit. The image data can be recorded on a memory card and displayed from that memory. The image sensing apparatus might be an electronic still camera.

The Kubo Reference

Kubo shows a photographing apparatus with two image sensors of different sizes. The apparatus includes interpolation units.

The Yoshihiro Reference

Yoshihiro shows an image pickup device in which when an image is displayed, power is supplied to the display circuitry and is cut to the image pickup element and the image processing components.

ARGUMENT

Claims 1-13

Claims 1-13 are directed to an image sensing apparatus which includes an image quality mode setting block for setting only one of a plurality of image quality modes, a solid state image sensing element for converting an optical image into an electric analog signal, and an AD conversion block for converting the analog signal output from the solid state image sensing element into a **single** digital signal with a quantization bit count corresponding only to the one image quality mode set by the image quality mode setting block.

The rejections of these claims contend that Nagano provides for setting only one image quality setting mode, supplied by selector 53. Assuming that to be so, nevertheless, selector 53 is not an AD conversion block which converts the analog signal into a single digital signal.

Further, Nagano's two AD converters do not convert the analog signal output from the solid state image sensing element into a single digital signal. Instead, they provide two digital signals, which therefore necessitate inclusion of selector 53. Accordingly, independent claim 1 and its dependent claims 2-13 distinguish patentably from Nagano and the other references

and are allowable.

Claims 14-25

Claims 14-25 are directed to an image sensing apparatus which includes an image quality mode setting block for setting one of a plurality of image quality modes, a solid state image sensing element for converting an optical image into an electric analog signal, and an AD conversion block for converting the analog signal into a digital signal. The AD conversion block has a plurality of quantization bit counts corresponding respectively to the plurality of image quality modes and is responsive to the image quality mode set by the image quality mode setting block to enable the quantization bit count corresponding to the set image quality mode and to disable the other quantization bit counts.

The rejections of these claims contend that Johnson has an image quality mode setting block which sets one of a plurality of image quality modes, and that Johnson teaches control of the AD converter in different quality modes. The rejection further contends that Johnson has an AD conversion block having a plurality of quantization bit counts corresponding respectively to the plurality of image quality modes, and that Johnson's AD conversion block is responsive to the image quality mode set by the image quality mode setting block to enable the quantization bit count corresponding to the set image quality mode and disable other quantization bit counts. These contentions are traversed.

Johnson's correlated double sampler and variable gain amplifier 44 amplifies the signal from the CCD sensor 14. The AD converter 46 converts this to a digital signal. Gain adjust circuit 47 then "performs the reverse operation of what is done in the VGA. For

example, if a gain of 8 is applied in the VGA, the gain adjust block shift [sic] the output by 3 bits to the right, thus performing a divide by 8 operation." See Johnson at column 4, line 66 to column 5, line 4.

There is no showing or suggestion of an AD conversion block having a plurality of quantization bit counts corresponding respectively to the plurality of image quality modes. Likewise, there is no showing or suggestion of the AD conversion block being responsive to the image quality mode to enable the quantization bit count corresponding to the set image quality mode and to disable the other quantization bit counts.

The Office Action repeatedly cites several lengthy passages from Johnson as supporting the various rejections. These have been reviewed, and the above responding arguments prepared. If the Examiner adheres to the rejection, the undersigned attorney requests a personal interview during which the Examiner is requested to specifically point out the particular wording in Johnson that supports the rejection.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including

extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: July 27, 2004

James N. Dresser, Esq.
Registration No. 22,973

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254